No. AN9301 April 1994

Application Note

HIGH CURRENT LOGIC LEVEL MOSFET DRIVER

Author: John Prentice

Introduction

Although the HV400 was designed as an interface between a pulse transformer and a power MOSFET, there are applications for high current MOSFET gate drive controlled by standard logic. This application note provides a method of interfacing the HV400 to logic signals. It also reviews the input control requirements of the HV400. The data sheet for the HV400 may be found in the “Intelligent Power IC’s” data book DB304.

HV400 Circuit Schematic

The HV400 schematic is shown in Figure 1. There are separate outputs for sinking and sourcing current. When the input goes low, resistor R3 provides base drive for Q2. An SCR is used to sink large currents. Transistor Q2 triggers SCR1 at both the anode and cathode gates. This triggering sequence begins as soon as D4 becomes reverse biased; the triggering delay time is then independent of the input fall time. Resistor R4 provides a base discharge path for Q1. Diode D6 increases the input hysteresis to reduce the chances that ringing at the input or output will trigger the SCR. Resistors R1 and R2 remove excess stored charge from the SCR and also help prevent false triggering. Diode D5 clamps the input low voltage.

A high input turns on Q1. Diodes D2 and D3, along with D1, prevent Q1 from saturating. Diode D1 also provides a means of passing charge from the input to the supply.

HV400 Input Characteristics

The HV400 is a non inverting current buffer. Pin 2 is the input control pin. For the output to be high, the input must also be high. This requires at least 12mA since R3 is approximately 1250Ω. Additional input current is required for the base current of Q1. The input driver should be capable of sourcing 200mA for a few hundred nanoseconds to achieve a 3A output current pulse but much less is required for smaller output currents due to the change in transistor gain with current and voltage. The input voltage should be 2V higher than the desired output voltage.

To set the output into the low state, the input voltage must drop 1V below the output. This can be accomplished by terminating the pin 2 input current since R3 acts as a pull-down resistor. The input voltage should be no more than 2V above pins 4 and 5 to make sure that Q1 will not turn back on.

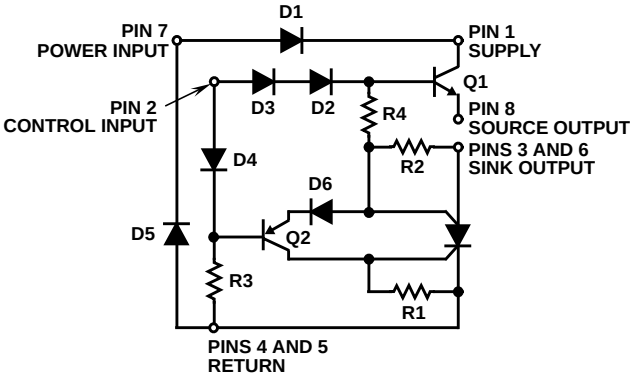


FIGURE 1. MOSFET DRIVER SCHEMATIC

Once the output is triggered low, it will remain low until the current into the output, pins 3 and 6, drops below 10mA and the SCR unlatches. The input must not go positive until the SCR unlatches and has had time to recover its voltage blocking capability defined by the “minimum off time” specification.

Logic Level Input

There are many instances where the control signal is a logic level referenced to the source of the MOSFET, i.e. logic ground and the source are at nearly the same potential. For example, forward, flyback and push-pull switch mode power supplies use power MOSFET’s with grounded sources.

The Intersil ICL7667 is a dual MOSFET driver that converts TTL/CMOS level signals into the higher voltages required for gate drives. The combination HV400 and ICL7667 results in a low cost, high output current, logic level input MOSFET driver. The circuit schematic is shown in Figure 2. One of the ICL7667 outputs becomes the input for the HV400 and the other is connected in parallel with the HV400 output. Since the ICL7667 is a CMOS product, its outputs swing rail-to-rail. Based on the HV400 input requirements, it should be apparent that a low impedance, high voltage (i.e. 15V) CMOS output is ideal for driving the HV400 input.

Copyright © Intersil Corporation 1993

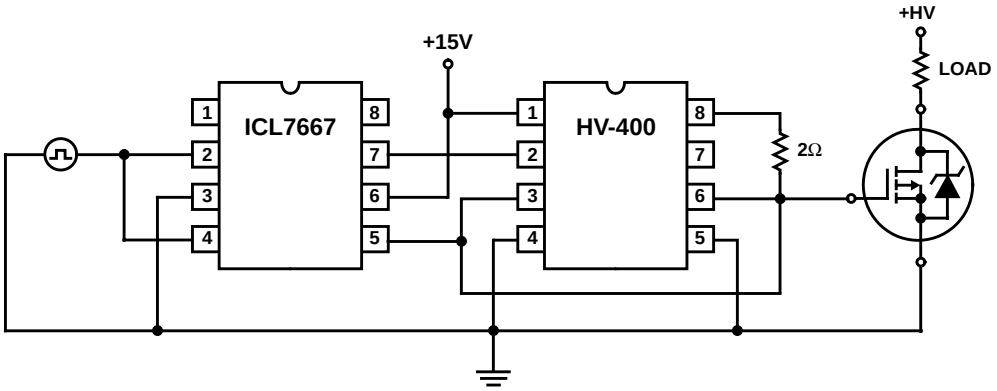


FIGURE 2. LOGIC LEVEL CIRCUIT

The result of combining one channel of the ICL7667 with the output of the HV400 is an improved driver with the voltage swing of a CMOS part and the large peak currents available from BiPolar. During switching transitions, the HV400 provides most of the sinking/sourcing current until the output is within 2V of the supply or ground. When the output is low, the ICL7667 continues to discharge the power MOSFET gate to ground after the HV400 SCR unlatches. It also provides a low impedance path to ground to keep the power MOSFET off in the presence of drain coupled noise or gate leakage currents. When the output is high, the ICL7667 continues to charge the MOSFET gate to the supply voltage minimizing MOSFET “on” resistance. Since most power MOSFET gate energy is dissipated in the HV400, the ICL7667 operates cooler minimizing the switching and delay times. The maximum supply voltage is 15V limited by the ICL7667.

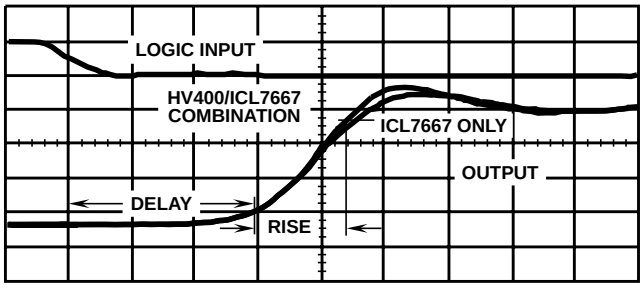
The following figures illustrate the performance of the HV400/ICL7667 combination. Figures 3 and 4 show the response with a 1nF capacitive load. Included for comparison is the response of the ICL7667 by itself. The low-to-high transition (Figure 3) has a 30nS delay and a 15nS rise time. The high-to-low transition (Figure 4) has a 10nS delay and a 14nS fall time. The HV-400 reduces the rise and fall times by only a few nanoseconds.

Figures 5 and 6 are for the same conditions except the load has been increased to 5nF. Here, the HV400 reduces the rise time to about 50% of that of the ICL7667 alone and the fall time is about 25%. The delay times are unchanged.

Figures 7 and 8 show the ICL7667/HV400 combination driving a 20nF load. From the dv/dt measurements, the peak source current is about $3^1/_3$A and the peak sink current is about 8A.

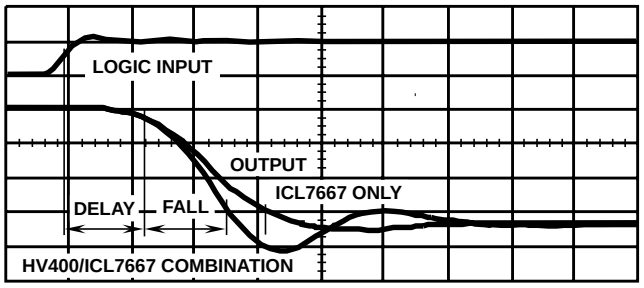
Summary

A simple circuit combination of the HV400 and an ICL7667 MOSFET drivers results in a logic compatible driver with large drive current capacity.



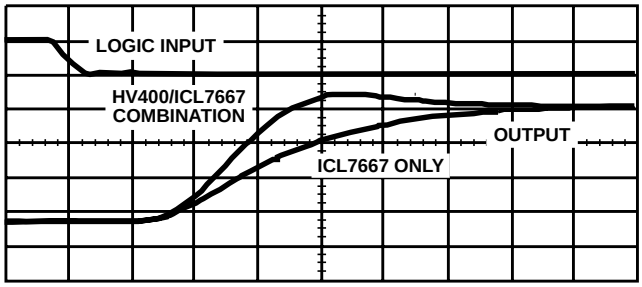
NOTE:
Input = 5.000V/div
Output = 5.000V/div
Timebase = 10.0ns/div
C_L = 1nF

FIGURE 3.



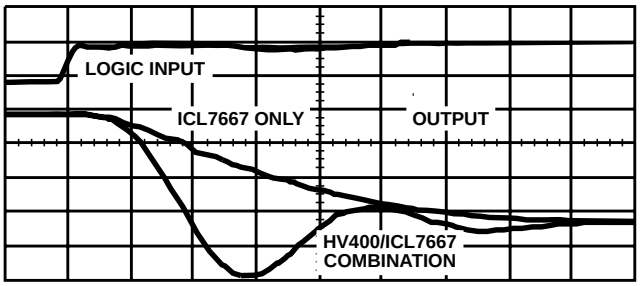
NOTE:
Input = 5.000V/div
Output = 5.000V/div
Timebase = 10.0ns/div
C_L = 1nF

FIGURE 4.



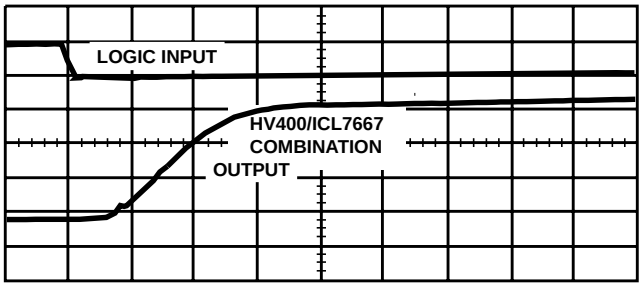
NOTE:
Input = 5.000V/div
Output = 5.000V/div
Timebase = 20.0ns/div
C_L = 5nF

FIGURE 5.



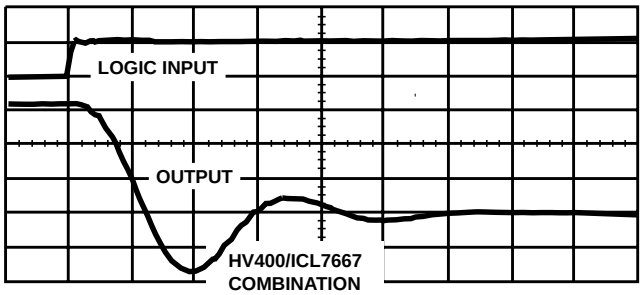
NOTE:
Input = 5.000V/div
Output = 5.000V/div
Timebase = 20.0ns/div
C_L = 5nF

FIGURE 6.



NOTE:
Ch. 1 = 5.000V/div
Ch. 2 = 5.000V/div
Timebase = 50.0ns/div
C_L = 20nF

FIGURE 7.



NOTE:
Input = 5.000V/div
Output = 5.000V/div
Timebase = 50.0ns/div
C_L = 20nF

FIGURE 8.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029